

OctaveRG400

Network Processor-Based 4-Port NGcN Switch

OctaveRG400 Specifications

- 4 half and full-duplex 10/100 Mbps ports
- MDC/MDIL: MII scan mode
- Wire-speed Layer 2/3 switching
- Wire-speed Layer 4 policy based switching
- 120-byte packet header lookup** → all field remarkable
- Address & policy lookup table embedded
- Packet buffer embedded
- 4K VLAN support
- IEEE 802.1Q support based on port, MAC, tag, subnet protocol
- Stacked VLAN (Q-in-Q)
- IGMP Snooping support
- Broadcast storm filtering
- Link Aggregation function -IEEE 802.3ad
- Management support: SNMP, RMON, SMON
- Flow control (IEEE 802.3x pause function)
- Loop resolution -STP (Spanning Tree Protocol), Rapid STP (802.1W), Per VLAN STP
- IPv6 switching, tunneling

L2/3/4 Performance, NAT, NAPT

- Wire-speed Layer 2/3 switching on all ports
- Wire-speed NAT/NAPT
- Wire-speed session detection and access control

Filtering

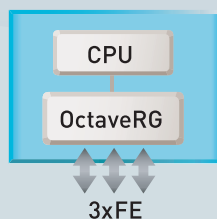
- MAC filtering, VLAN filtering, IP filtering
- TCP/UDP Port filtering, DHCP snoop/ARP snoop filtering
- NetBIOS, NetBEUI filtering, NBT (NetBIOS over TCP) filtering
- IPX socket number filtering
- Filtering rules can be added if necessary

QoS All Features Covered

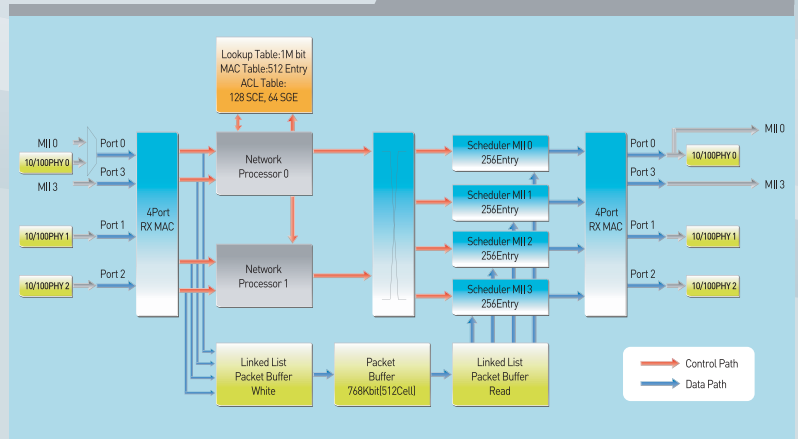
- ACL (access control list)
 - L1: Physical Port
 - L2: Destination MAC address
Source MAC address
Ethertype COS
VLAN ID
 - L3: Source IP address
Destination IP address
TOS
Protocol ID
 - L4: Source port number
Destination port number
- NetBIOS/NetBEUI, value/mask, range
unicast MAC, unknown MAC, multicast MAC,
broadcast MAC, unicast IP packet, multicast IP packet
- ACL Output
Remarking, VLAN ID insert, filtering, port redirection, port mirroring, CPU redirection, CPU mirroring
- Prioritization
L2 CoS, L3 IPv4 TOS, L3 IPv4 DSCP, L3 IPv4 IP-precedence packet type (unicast/multicast), IPv6 TC
- Policing
Granularity, token bucket, priority based
multi-stage policing, operation position,
port based policing, flow based policing
- Shaping -granularity 100Kbps
- Scheduling
SPQ, DWRR and combination
- Bandwidth limiting -token bucket
: min. 1ms, max. 1s
- Rate control support



System Architecture



BLOCK DIAGRAM



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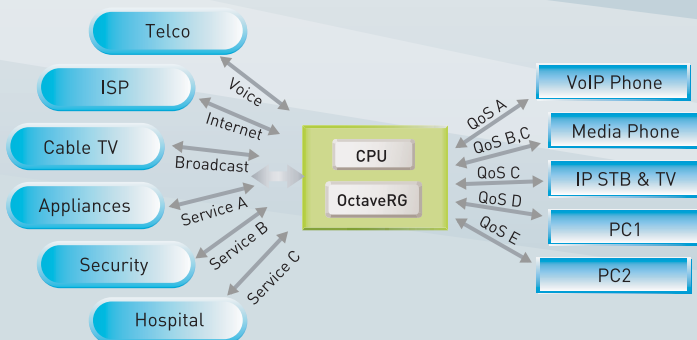
Network Processor Support Features

- Flow-based QoS: filtering, CoS remarking, ToS remarking, VLAN insert/delete, port mirroring, CPU redirection, per-flow bandwidth limiting
- BPDU/PAUSE control packet processing
- Broadcast/multicast storm filtering
- 3 kind of DLF (destination lookup fail) policy -2DLF, 3DLF, MDLF
- Port-/Tag-based VLAN -4096 entries
- IP forwarding -512 entry
- NAT forwarding -2048 entry
- Port-forwarding (static NAT)
- Multicast forwarding -256 entries
- IPv6 switching
- IGMP snooping
- Q-in-Q processing

Applications

- RGW (residential gateway), or IAD (integrated access device)
- AP (access point) with perfect NAT/NAT and QoS
- Switch/router for SME: SOHO switch/router, IP sharer
- Metro Ethernet switch: MPLS LES (Label Edge Switch)
- FTTH EPON switch: ONU/ONT
- IPv6 switch/router, NGcN switch

Home/SOHO/SME Gateway Switch for IP Convergence Network



QoS Enhancement Features

- Hardwire 128 classification/ACL rules for 12-tuple
 - physical port
 - des. MAC
 - src. MAC
 - COS
 - VLAN ID
 - Ethernet type
 - TOS
 - protocol ID
 - src. IP
 - des. IP
 - src. Port
 - des. Port
- (128 x n) classification/ACL rules defined by Packet Processor after hardwire classification
- Minute per-flow bandwidth control: Flow-level bandwidth metering by a Packet Processor. Flows are defined for any combination of 12-tuple
- VOQs (virtual output queues): Each flow's service policy is determined respectively in reference to output queue status.
- Priority remarking based on:
 - User priority bits of VLAN tag
 - Ether Type field value
 - TOS field value of IPv4 header
 - Flow label field value of IPv6 header
 Prioritized packets assigned to 4 priority queues.
- Mixed scheduler of strict priority queuing and deficit weighted round robin (DWRR) with 4-level priority

Interfaces

- 1xMII + 3xPHY or 2xMII + 2xPHY
- SPI/8bit Local bus for CPU
- MDC/MDIO

Device Specifications

- Package: 128-QFP
- Fabrication: CMOS 0.18 μ
- Power Supply: 1.8V Core, 3.3V I/O
- Power Dissipation: Typical 1.1W
- System Clock: 125 MHz